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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,549	01/18/2000	Korbin Van Dyke	01000.9901080	9816
29153	7590	11/28/2006	EXAMINER	
ATI TECHNOLOGIES, INC. C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C. 222 N.LASALLE STREET CHICAGO, IL 60601			VO, LILIAN	
			ART UNIT	PAPER NUMBER
			2195	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/484,549

Applicant(s)

DYKE ET AL.

Examiner

Lilian Vo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2 - 12 and 15 - 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2 - 12 and 15 - 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 2-12 and 15- 21 are presented for examination. Claims 1, 13 and 14 have been cancelled.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Applicant is advised that should claim 15 be found allowable, claim 18 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2 – 12, 15 – 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Bonola (USPN 5,706,514).

6. As per **claims 15 and 18**, Bonola teaches the invention as claimed, including a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising:

queuing tasks (col. 3 lines 61-65);

identifying available processing resources in the homogeneous multiprocessor environment independent of the tasks (col. 7 lines 36 - 38, 42 – 52 and 57 – 61);

allocating the available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment and the processing requirements of each of the tasks (col. 7 lines 42-52; col. 8 lines 11-13);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 8, lines 13 – 18); and

performing the tasks using the available processing resources to produce resulting data (col. 9 lines 13-23), wherein the functional programs cause the available processing resources to perform the tasks of at least one of: graphics image processing, video processing, audio processing and communications processing (col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

7. As per **claim 2**, Bonola teaches the invention as claimed, including the method of claim 15 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set (col. 2 lines 6-10; col. 3 lines 37-44).

8. As per **claim 3**, Bonola teaches the invention as claimed, including the method of claim 2 wherein the first instruction and the second instruction share an identical bit pattern but perform different operations (col. 1 lines 15-26).

9. As per **claim 4**, Bonola teaches the invention as claimed, including the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set (col. 3 lines 26-35; col. 7 lines 22-33).

10. As per **claim 5**, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second instruction set (col. 8 lines 31-45).

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11. As per **claim 6**, Bonola teaches the invention as claimed, including the method of claim 3 wherein the tasks comprise x86 processing (col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

12. As per **claim 7**, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

receiving the initial data from a first input/output device (col. 8 lines 11-15).

13. As per **claim 8**, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

passing the resulting data to a first input/output device (col. 9 lines 13-23).

14. As per **claim 9**, Bonola teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises the step of:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (col. 9 lines 13-23).

15. As per **claim 10**, Bonola teaches the invention as claimed, including the method of claim

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9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (col. 8 lines 46-65).

16. As per **claim 11**, Bonola teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (col. 9 13-15, 19-23).

17. As per **claim 12**, Bonola teaches the invention as claimed, including the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted (col. 8 lines 46-65).

18. As per **claim 16**, Bonola teaches the invention as claimed, including the method of claim 15, further comprising:

keeping track, remotely from the resources, of the capabilities of all available processors of the homogeneous multiprocessor environment (col. 7 lines 42-52); and

identifying, independent of the tasks, available processing resources in the homogeneous multiprocessor environment based solely on the capabilities kept track of remotely (col. 7 lines 36-38, 42-52).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

20. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola (USPN 5,706,514).

21. As per **claim 17**, Bonola teaches the invention as claimed, including an apparatus comprising:

a plurality of processors coupled to a bus (col. 4 lines 29-33; Fig. 1);

an input/output interface coupled to the bus (col. 4 lines 52-54; Fig. 1);

a plurality of input/output devices coupled to the input/output interface (col. 4 lines 52 - 57, Fig. 1), the plurality of processors processing program code configured to perform a plurality of tasks (col. 9 lines 24-27), the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with a first input/output device of the plurality of input/output devices (col. 7 lines 22-25);

program code configured to cause a second portion of the plurality of processors to interact with a second input/output device of the plurality of input/output devices (col. 7 lines 42 - 52);

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program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 8 lines 11-18);

wherein the first portion of the plurality of processors provides functionality as found in a first application-specific subsystem and wherein the first input/output device is the first application-specific subsystem (col. 3 lines 23-30); and

wherein the second portion of the plurality of processors provides functionality as found in a second application-specific subsystem and wherein the second input/output device is the second application-specific subsystem (col. 7 lines 42-52; col. 8 lines 11-18); and

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode (col. 3 lines 26-35; col. 7 lines 22-33; col. 8 lines 11-18).

With respect to the limitation of kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode, Bonola discloses “a technique for handling processor mode mismatched instructions or commands encountered by a CPU within multiprocessor computer system...if a multimode processor encounters a command or instruction that it cannot execute without shifting modes or mode emulation, it will look for an alternate processor present in the computer system to instead handle the mode mismatched command...” In other words, Bonola’s system can perform the resource allocation among the processors regardless of a processor mode. Thus, the limitation narrowed by the claim is considered obvious over Bonola since applicant has not disclosed that limitation solves any stated problem or is for any particular purpose and it appears that Bonola’s system is capable of perform the functions as claimed equally well. Therefore, it

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would have been obvious to one of an ordinary skill in the art, at the time the invention was made to utilize the features as disclosed by Bonola to perform the tasks as desired.

22. Claims 19 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola (USPN 5,706,514) as applied to claims 15, 16 and 18 above, in view of Sinibaldi et al. (US 6,338,130, hereinafter Sinibaldi).

23. Regarding **claim 19**, Bonola discloses the step of allocating the available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment comprises allocating the available processing resources among the tasks based on the ability of each of the available processors of the homogeneous multiprocessor environment (col. 7 lines 36 – 38, 42 – 52, 57 – 61, col. 8 lines 11 – 18, 46 - 65 col. 9 line 12 – 23). Bonola did not clearly disclose the availability of each available processors to be divided or aggregated with another processor to provide a processing resource. Nevertheless, Sinibaldi disclose the step of allocating the available processing resources among the tasks based on the capabilities of each of the available processors comprises allocating the available processing resources among the tasks based on the ability of each of the available processors to be divided or aggregated with another processor to provide a processing resource (col. 12 lines 59 – col. 13 line 5, lines 28 – 46, col. 19 lines 40 – 52). Therefore, it would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate Sinibaldi's teaching together with Bonola to makes optimal use of the available processing capability of the processors at all time (Sinibaldi: col. 13 lines 45 – 46).

24. **Claims 20 – 21** are rejected on the same ground as stated in claim 19 above.

Response to Arguments

25. Applicant's arguments filed 9/12/06 have been fully considered but they are not persuasive for the reasons set forth below.

26. Regarding applicant's remark that Bonola does not teach and/or suggest the limitation "identifying available processing resources in the homogeneous multiprocessor environment independent of the tasks" (page 11, 2nd paragraph), the examiner disagrees. First, Bonola clearly teach the step of identifying the available processing resource in col. 7 lines 36 – 38, 42 – 52 and 57 – 61 in which "a determination is made whether a slave CPU 21 – 23 is available ...". Second, it's the office understanding and/or interpretation that a separate process other than the tasks is performing the step of identifying, which is exactly what Bonola discloses.

If applicant believes these citations do not disclose such teaching or provide proper meaning of the claimed invention, applicant must provide a clear definition and the location of these limitations in the specification. Further, while it is appropriate to use the specification to determine what applicants intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation. A broad interpretation of a claim by Office personnel will reduce the possibility that the claim, when issued, will be interpreted more broadly than is justified or intended. Applicants can always amend a claim during prosecution to better reflect the intended scope of the claim.

27. Regarding applicant's remark that applicant unable to find any teaching or suggestion in the cited portions of Bonola where tasks are performed and wherein the functional program cause the available processing resources to perform the tasks of at least one of: graphics imaging processing, video processing, audio processing and communications processing (page 11, 2nd paragraph), the examiner submits that these features are merely a recitation of the intended use of the claimed invention. Such an intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. By loading a processor with the information necessary to proceed with processing of a particular task, the processors may perform any of graphics image processing, video processing, audio processing, or communications processing.

Therefore, applicant is directed to col. 3 lines 26 – 35 and fig. 1 in which Bonola discloses the processors execute an input/output kernel program and the processors communicate with input output devices 62, 68, 71, etc. One of an ordinary skill in the art would recognize that based on such disclosure, *at least the communication processing task is inherently being performed by the processor*. Claim language recites that *at least of the task* are to be performed. Thus, the reference is required to show only one type of task in this case which is communication processing then it meets the claim.

28. With respect to applicant's remark that "graphics image processing... and/or communications processing may be performed on a system and not specifically a processor or

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processing resource” (page 13 2nd paragraph), the examiner disagrees. An ordinary skill in the art would recognize that a system also includes a processor. Thus, an x86 system would necessarily include an x86 processor in order for it to function accordingly.

With respect to applicant’s remark that “the Office Action’s assertion runs afoul of Applicant’s written description” (page 13 3rd paragraph), applicant to note that the examiner assertion is based on Bonola’s disclosure and the knowledge of one of an ordinary skill in the art. Furthermore, prior art Brown et al. (US 6,381,321) discloses a telecommunication system with x86 processor that is capable of processing communication tasks and/or video processing (col. 3 line 13 – 16 and col. 7 lines 1 – 3).

29. Regarding applicant’s remark that Bonola does not teach and/or suggest the limitation of claims 2 and 3 (page 14 last paragraph), the examiner disagrees. Bonola discloses such features in col. 1 lines 15 – 26, col. 2 lines 6 – 10 and col. 3 lines 37 – 44. Bonola’s system is capable of performing different tasks and/or operations in the same system. Thus, the instructions to perform such tasks are inherently share an identical bit pattern because they are able to function and/or operate sufficiently within the system.

30. With respect to applicant’s remark that “it is clear that Bonola’s system always considers the processor mode to determine what processor within a multiprocessor computer system should execute the command or instruction” (page 16 1st paragraph), applicant to note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from

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the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Furthermore, the operation based on the processor mode as discussed in Bonola does not mean the claims are patentable distinct over the prior art. Although applicant's specification did not mention the execution is under any type of the processor mode, one of an ordinary skill in the art would recognize that applicant's processors has to be functioned in some type of mode. As noted above, Bonola's system can perform the resource allocation among the processors regardless of a processor mode. Thus, the limitation narrowed by the claim is considered obvious over Bonola since applicant has not disclosed that limitation solves any stated problem or is for any particular purpose and it appears that Bonola's system is capable of perform the functions as claimed equally well. Therefore, it would have been obvious to one of an ordinary skill in the art, at the time the invention was made to utilize the features as disclosed by Bonola to perform the tasks as desired.

31. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (page 16 1st paragraph), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

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32. In response to applicant's argument that the examiner mischaracterizes the teaching from Bonola in attempt to read on applicant's claim language (page 16 1st paragraph), the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lilian Vo
Examiner
Art Unit 2195

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November 22, 2006


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